

| Course Number | COE328 |
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| Course Title | Digital Systems - F2022 |
| Semester/Year | Fall 2022 |
| Instructor | Shazzat Hossain |
| TA Name | Sajjad |

| Lab/Tutorial Report No. | Lab 1 Part 1 |
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| Report Title | **Introduction to CAD tools** |
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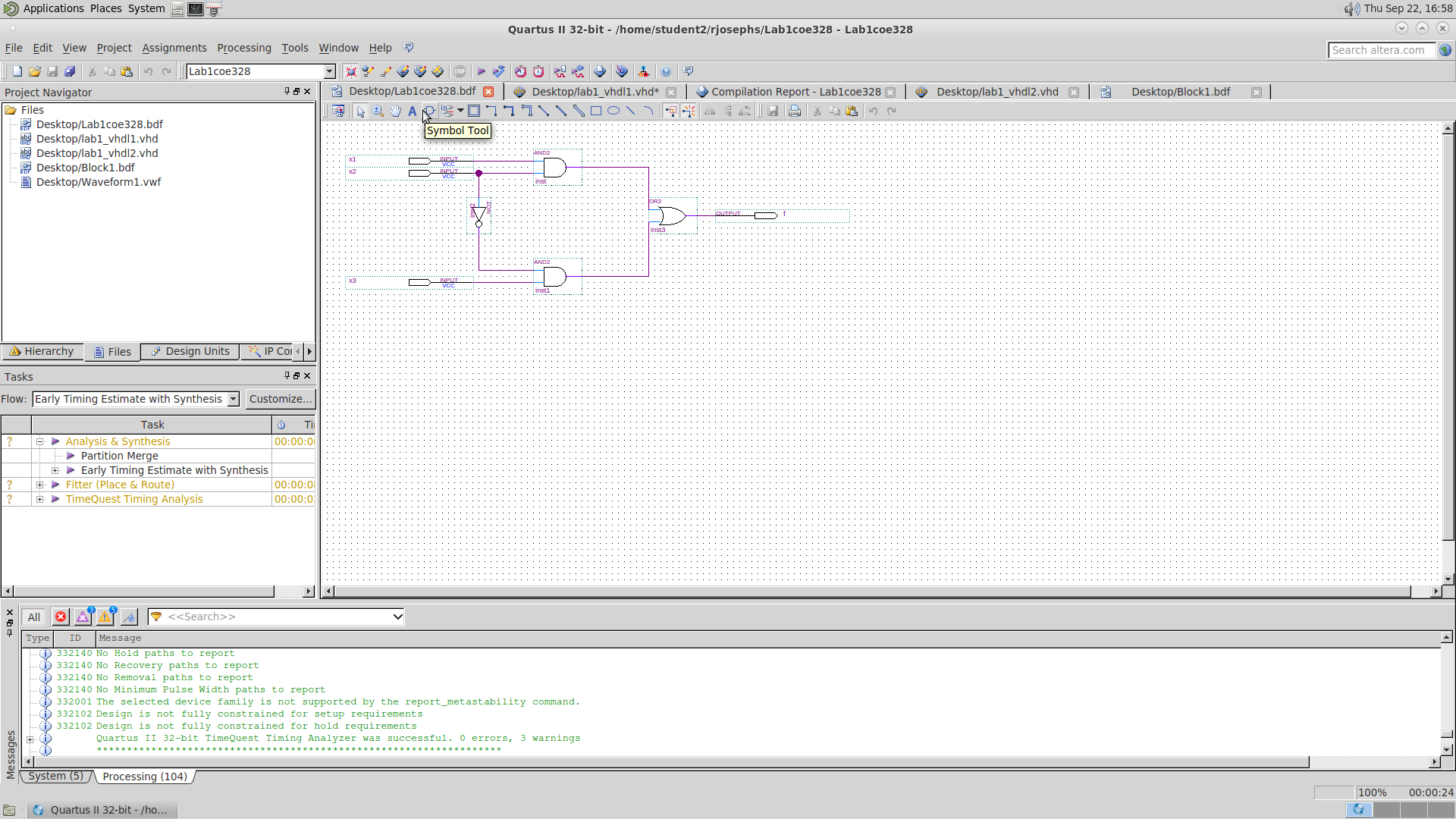
| Section No. | 11 |
| --- | --- |
| Group No. | N/A |
| Submission Date | Sept 23, 2022 |
| Due Date | Sept 25th, 2022 |

| Student Name | Student ID | Signature\* |
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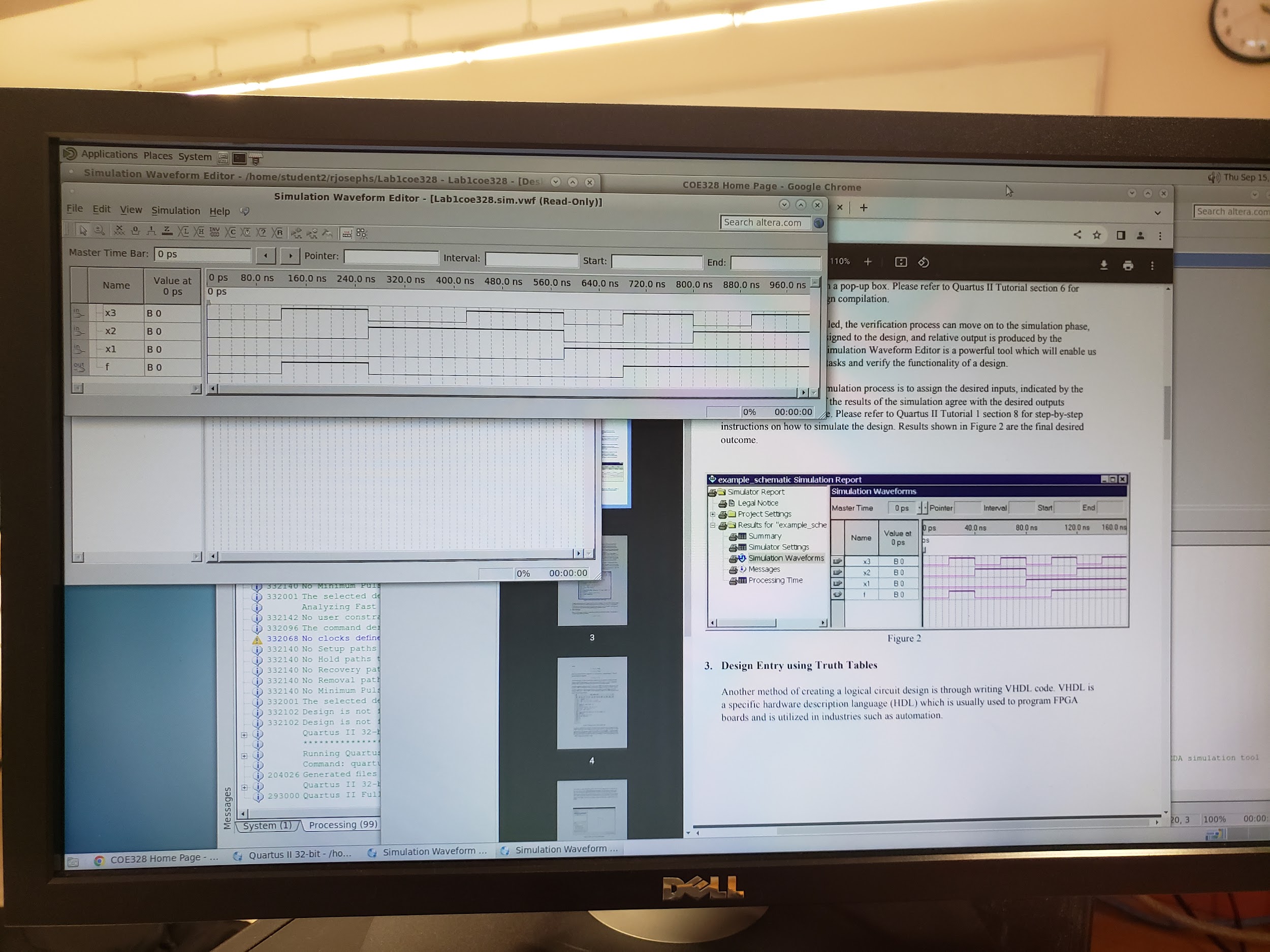
[*http://www.ryerson.ca/content/dam/senate/policies/pol60.pdf*](http://www.ryerson.ca/content/dam/senate/policies/pol60.pdf)

**Schematic Design:**



- This is a picture of our first schematic design created on week one of our lab using Block Editor tool in Quartus II 13.0.

**Waveform Simulation Diagram:**



- This is a picture of our First simulation/waveform results created on week one of our lab 1 using the Block Editor tool in Quartus II 13.0.

**Conclusion:**

To wrap up our lab 1 part one, we observed a method of creating a logical circuit design through boolean algebra and truth tables. In this method, a schematic design was created with the block editor tool in Quartus II 13.0 using logic gates. The schematic design was made just like figure one in the lab manual, which has three input pins connected in between two AND gates interconnected to an OR gate, giving us an output f. We then compiled the design and created a waveform vector file to perform wave simulations on the design. Then introduced values for the input ports and created the waveform design. Once the waveform designs were created according to the lab outline figure 2, we compiled the waveform, giving us a waveform output f for the mixed design.